

# ***LVDS Serdes 48 EVM Kit Setup and Usage***

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## **Abstract**

This document describes the Texas Instruments (TI™) LVDS Serdes 48 evaluation module (EVM) kit. The LVDS Serdes 48 EVM kit is used to evaluate and design high data throughput prototypes using the TI LVDS95 transmitter and LVDS96 receiver boards. The boards allow the designer to connect 21 bits of data and clock to the transmitter board where LVDS technology is available to serialize and transmit the data along four differential pairs (three data and one clock). The receiver board then deserializes the data, providing 21 bits of 3.3 V TTL data and clock.

The transmitter and receiver boards can be used to evaluate device parameters while acting as a guide for high-speed board layout. The high-speed LVDS interface uses a 50  $\Omega$  controlled-impedance parallel cable available in various lengths. The low-speed interface uses a standard 50 pin parallel ribbon cable. Overall, the designer can use the EVM kit as a tool for successful evaluation and design of an end product.

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## Introduction

The TI LVDS Serdes 48 EVM kit is used to evaluate and design high data throughput prototypes using the TI LVDS95 transmitter (TX) and LVDS96 receiver (RX) boards. The boards allow the designer to connect 21 bits of TTL-compatible data and clock to the transmitter board where LVDS technology is used to serialize and transmit the data along four differential pairs. The receiver board then deserializes the data, providing 21 bits of TTL data and clock.

The transmitter and receiver boards can be used to evaluate device parameters while acting as a guide for high-speed board layout. The LVDS Serdes EVM boards can be used as daughter boards that are plugged into new or existing designs.

As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to 50  $\Omega$  for the high-speed LVDS serial connections and 75  $\Omega$  for the slower parallel data. In addition, the 50  $\Omega$  impedance mismatches are reduced by designing the component pad size to be as close as possible to the width of the connecting transmission line. Vias are minimized and, when necessary, placed as close as possible to the device drivers. Since this is a combined serial and parallel interface, care was taken to control both impedance and trace length mismatch (board skew).



Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission line effects are crucial when designing high-speed boards.

Some of the advanced features offered by this board include:

- PCB (printed circuit board) and LVDS cable are designed for high-speed signal integrity.
- Flexibility—The PCB can be configured for additional signals and power supply options.
- Provision for chassis-mount connector provides for a low EMI interface.
- All input/output signals are accessible for rapid prototyping.
- Power can be supplied through either the 50 pin IDC ribbon cable or a screw-on wire crimp connector.
- Series termination resistors provide parallel RX outputs.

## LVDS Serdes 48 EVM Kit Contents

- LVDS Serdes 48 transmitter board (SN65LVDS9TXEVM)
- LVDS Serdes 48 receiver board (SN65LVDS9RXEVM)
- LVDS Serdes 48 EVM kit documentation

## LVDS Serdes 48 EVM Boards Configuration

The LVDS Serdes 48 EVM boards give the developer various options for operation, many of which are selectable by jumpers. Other options can be either soldered into the EVM or connected through input connectors.

The 50 pin IDC connector provides a connection for both power and data signals. Header "P3" provides access to the signals not used in the 3M Mini D Ribbon (MDR) cable. The "P4" header on the transmitter board is used to select power sources for the voltage regulator and optional input power. The power plane is split for both the transmitter and receiver. Therefore, jumpers labeled "Vcc Sel" are used to connect the chip power plane to the desired voltage source. Additional jumpers are provided for chip enable and output power. For details, see Figure 8, "LVDS Serdes 48 Pin Transmitter Schematic," and Figure 9, "LVDS Serdes 48 Pin Receiver Schematic" in Appendix A.

The board is normally delivered in a default configuration that requires external clock and data inputs. Power can be supplied either through the 50 pin IDC connector or through a 4 pin connector (TB1). The LVDS Serdes 48 EVM is shipped with jumpers for default operation. Table 1 and Table 2 show the default configurations.



Table 1. Default Transmitter Board Configuration as Shipped

Designator	Function	Condition
TB1	Alternate power	Another means of providing power to or from the TX board
P4	+12 VS – +12 VL Peripheral power source	Jumper installed between Pins 1 and 2 <Optional – Not necessary for EVM function>
P4	+5 V – VR IN Normal TX power	Jumper installed between Pins 3 and 4 <Normal power input for VR or board>
P6	Vout SEL	Jumper installed between Pins 1 and 2 (Vout : +3.3 V)
P7	TX Vcc SEL	Jumper installed between Pins 1 and 2 (Vcc : +3.3 V)
P3	3.3 V Aux Out	Jumper installed between Pins 20 and 18 (T9 : +3.3 V)
P3	12 V Power Output Select	Jumper installed between Pins 1 and 2 (T1 : +12 V)
P3	12 V Power Output Select	Jumper installed between Pins 5 and 6 (T3 : +12 V)
P7	TX Vcc SEL Selects power source for RX chip	Jumper installed between Pins 1 and 2 (Vcc : +3.3 V)
P5	SHTDN SEL	Jumper installed between Pins 2 and 3

Note: For details, see Figure 8, “LVDS Serdes 48 Pin Transmitter Schematic,” in Appendix A.

Table 2. Default Receiver Board Configuration as Shipped

Designator	Function	Condition
TB1	Alternate Power	Another means of providing power to or from the RX board
P3	12 V Power Input Select Peripheral power source	Jumper installed between Pins 1 and 2 <Optional – Not necessary for EVM function>
P3	12 V Power Input Select Peripheral power source	Jumper installed between Pins 5 and 6 <Optional – Not necessary for EVM function>
P3	3.3 V Alternate input source	Jumper installed between Pins 19 and 20 <Optional – Not necessary for EVM function>
P4	Vout Sel Alternate output source	Jumper installed between Pins 1 and 2 <Optional : +3.3 V RX power output>
P5	SHTDN SEL Enables/Disables RX	Jumper installed between Pins 2 and 3 < Enables RX chip U1>
P6	RX Vcc SEL Selects power source for RX chip	Jumper installed between Pins 1 and 2 (Vcc : +3.3 V)

Note: For details, see Figure 9, “LVDS Serdes 48 Pin Receiver Schematic,” in Appendix A.

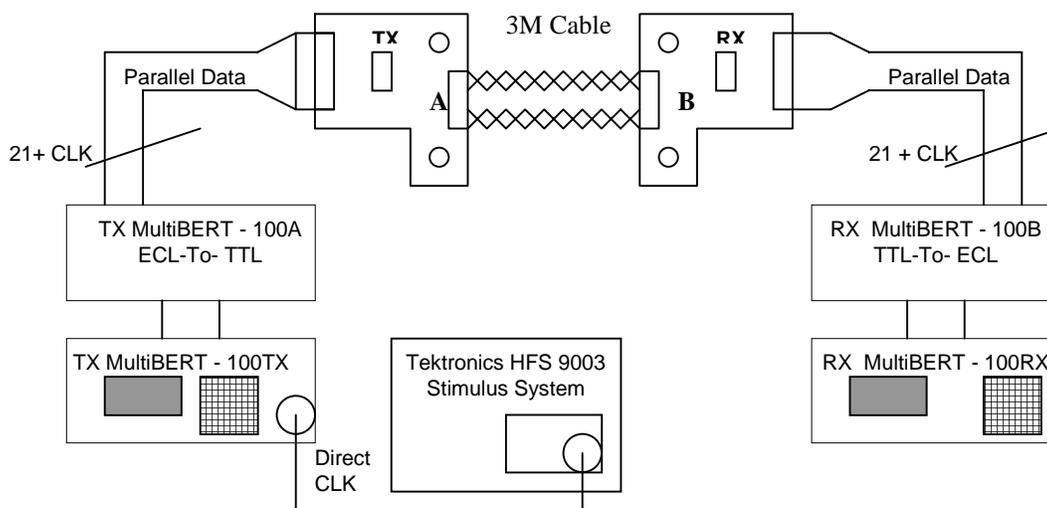
## Typical Test and Setup Configuration

The following typical configuration is used to test the LVDS Serdes transmitter and receiver pair. A parallel bit error rate tester (BERT) generates a predefined parallel bit pattern. The pattern is connected to the transmitter board through a 50 pin IDC connector to the TX chip. The TX chip serializes the data and transmits the data using LVDS technology through the MDR cable (see Appendix A). The RX chip then converts the serial data back to parallel TTL compatible data. The data is then received by the BERT and compared against a predefined pattern.

If any bit errors are received, a bit rate is displayed over the time interval of the test. Therefore, the BERT test is a good indication of failure rate. However, the test does not give the designer an indication of timing margin to bit failure.

The BERT test configuration can also be used to measure the system's characteristic eye diagram on the high-speed LVDS side at test point "B". The eye opening is a direct indication of how much margin exists before the system starts to develop bit errors. During the eye characterization, a pattern of Pseudo Random Binary Sequence (PRBS) is sent through the system.

Figure 1. LVDS Serdes 48 EVM Test Configuration



## Test Results

The EVM boards were tested to verify system performance. These tests are useful in showing the capabilities of the system and both TX and RX LVDS Serdes 48 devices.

The first test performed was the BERT test, which was run using PRBS pattern. Figure 1 shows the setup configuration. This test shows the bit errors relative to the time the system is running. The longer the test is run the greater the probability of a bit error. The BERT test was operated for 30 minutes at 65 MHz, nominal 3.3 volts Vcc and across 5 meters of LVDS cable. The test showed no bit errors over the 30 minutes of operation.



The second test shows eye timing characteristics of the high-speed LVDS portion of the system. An eye diagram is used to evaluate design and timing margins of the system. Eye closure is a result of intersymbol interference and additive noise that is directly proportional to cable quality and length. Therefore, it is important to the designer to keep the eye as open as possible to prevent bit errors from occurring.

In Figure 2 through Figure 7, the eye closes as the cable length increases. This is especially true of the 10-meter cable at 65 MHz. As clearly shown in Figure 2 and Figure 4, the 10-meter cable exhibits a much smaller eye than the 2 meter cable. In addition to cable length, the frequency of operation can directly affect the eye's opening. As the period increases, the margin increases for deterministic jitter and noise in the system. Thus, a system designer can use a longer cable at a lower frequency. This can be seen in Figure 4 and Figure 7, where the eye at 65 MHz is much smaller than the eye at 40 MHz.

Figure 2. Eye Diagram Taken RX(B) Across 2 m of Cable at 65 MHz

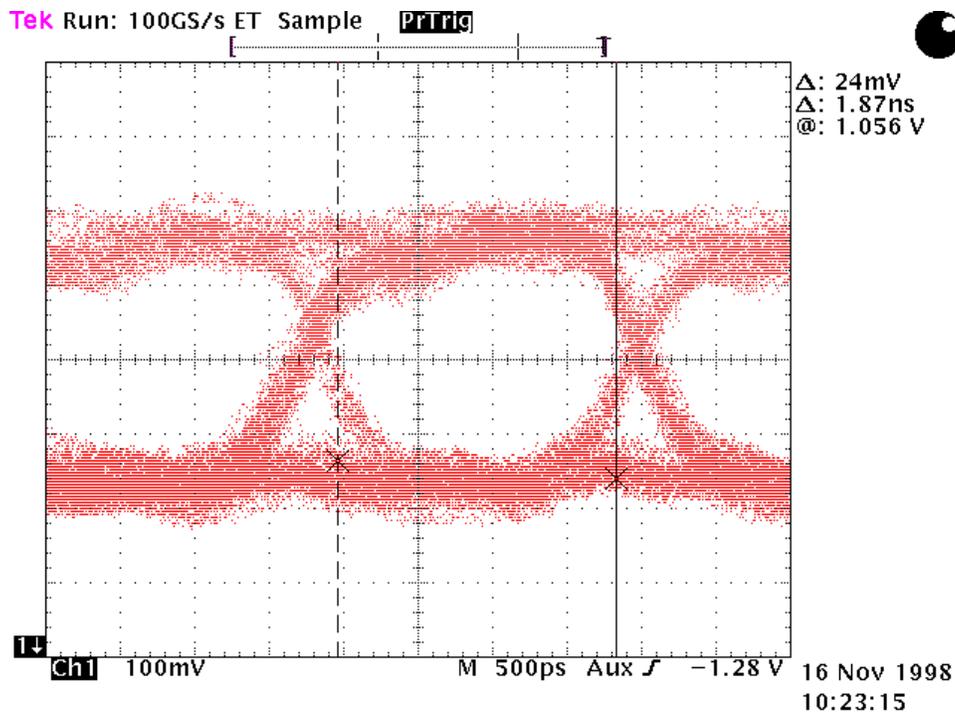




Figure 3. Eye Diagram Taken RX(B) Across 5 m of Cable at 65 MHz

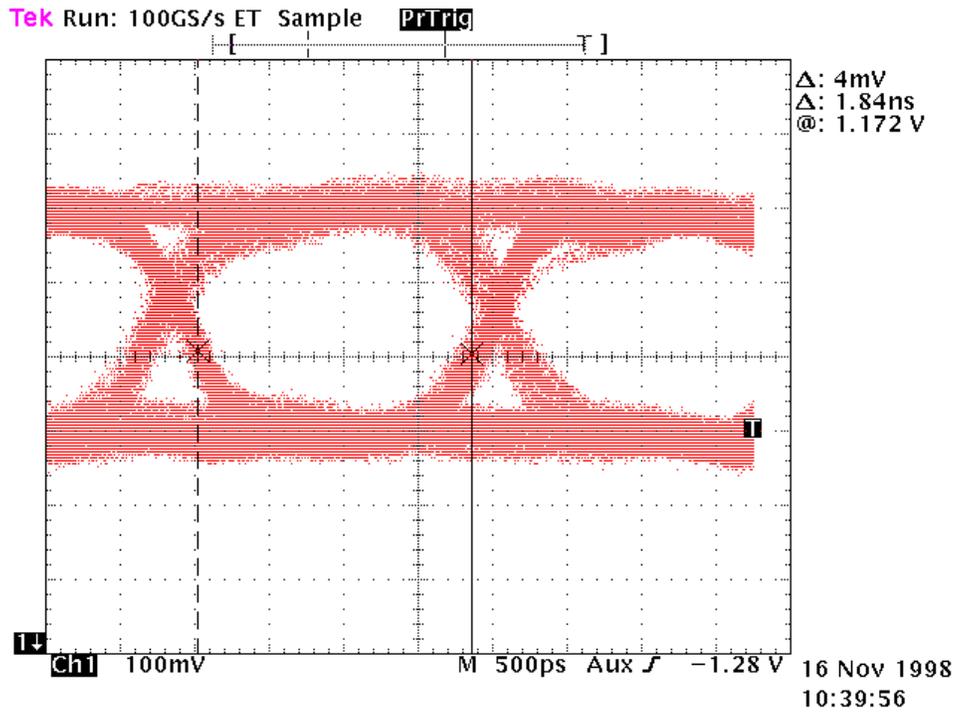


Figure 4. Eye Diagram Taken RX(B) Across 10 m of Cable at 65 MHz

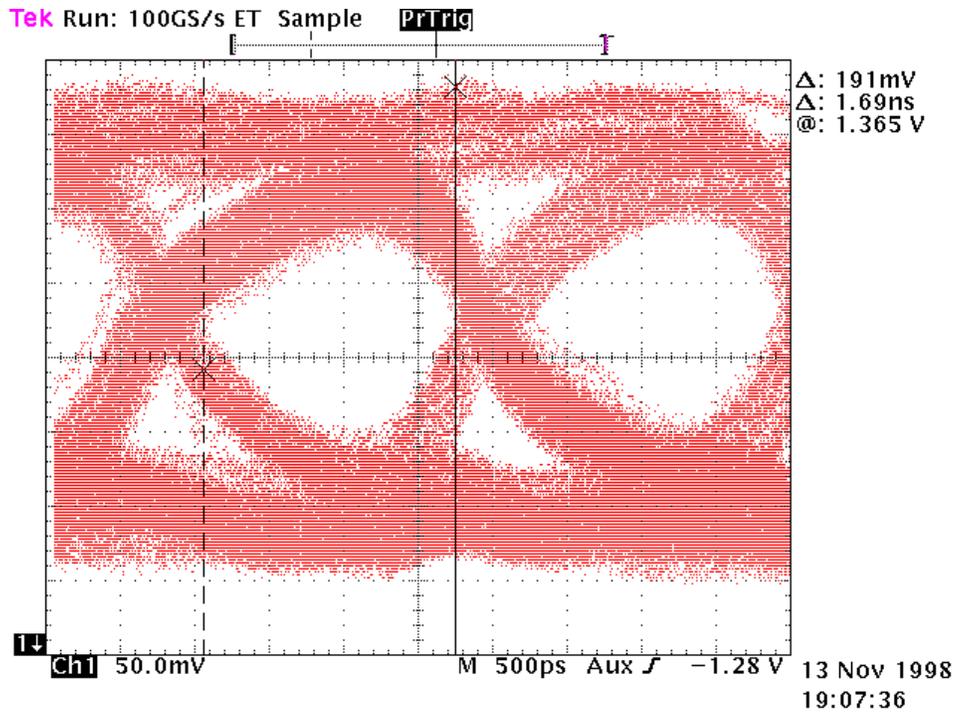




Figure 5. Eye Diagram Taken RX(B) Across 2 m of Cable at 40 MHz

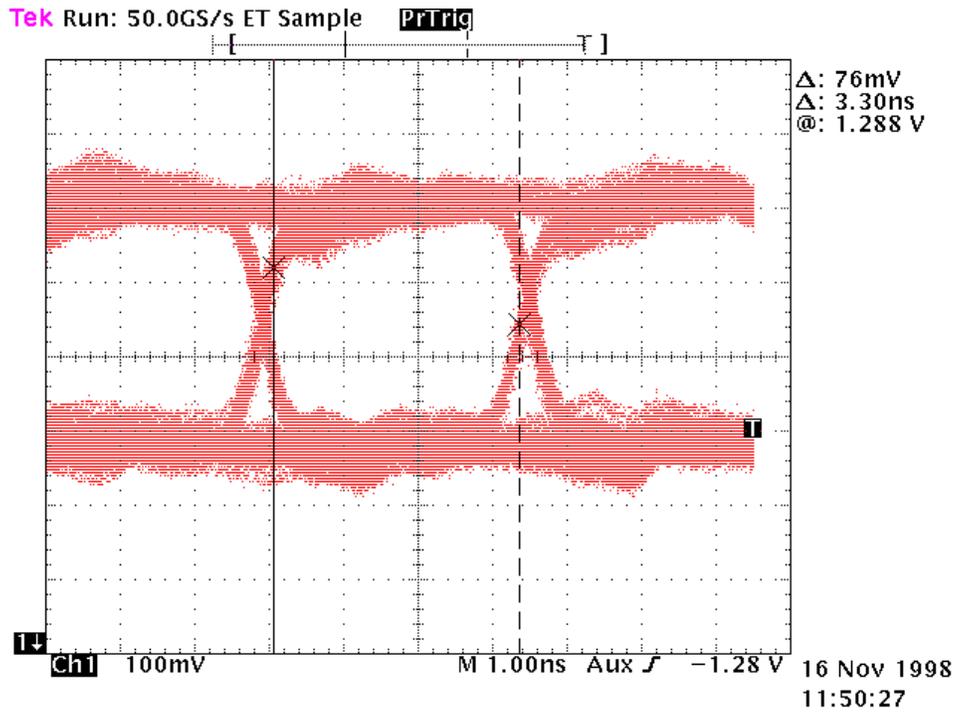


Figure 6. Eye Diagram Taken RX(B) Across 5 m of Cable at 40 MHz

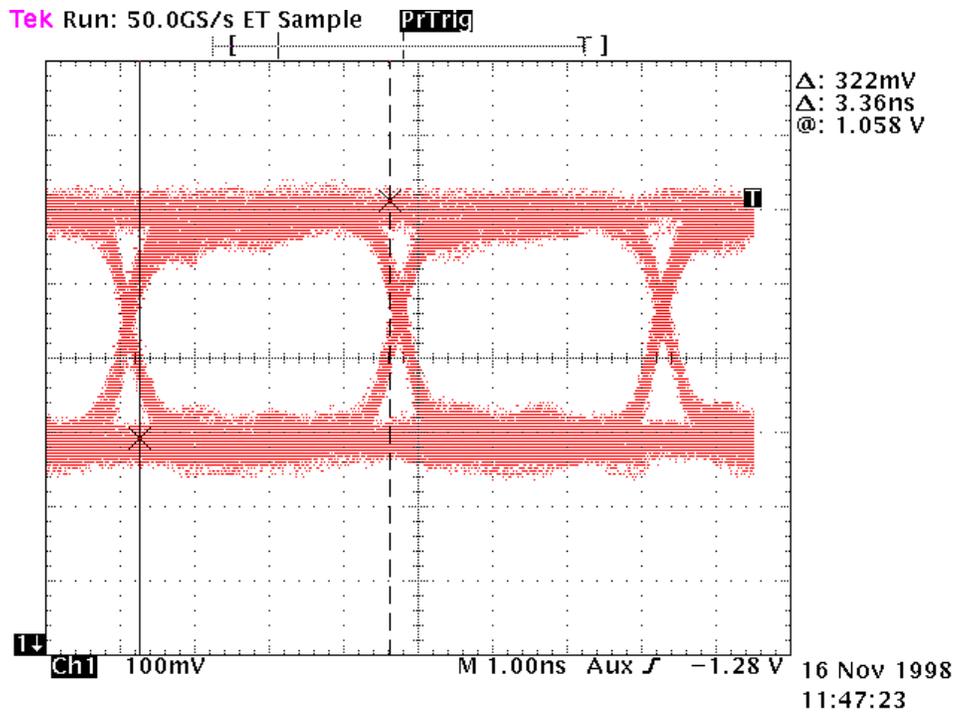
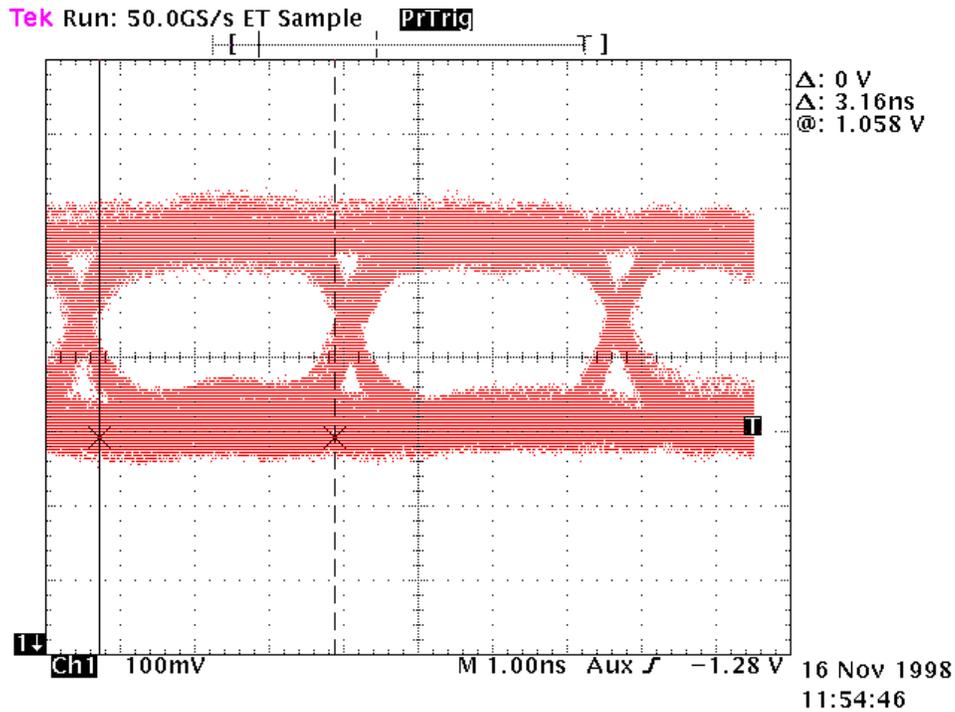




Figure 7. Eye Diagram Taken RX(B) Across 10 m of Cable at 40 MHz



## PCB Transmission Line Characteristics

The PCB characteristics are calculated and based on the layer construction and trace width of the board. This should be useful in determining the proper interface to the EVM and establishing system timing.

Table 3. LVDS Serdes 48 Transmitter PCB Transmission Line Characteristics

Device Pin No.	Connector Pin No.	Trace Width (inches)	Length (inches)	Capacitance (pF)	Inductance (nH)	Impedance (Ω)	Line Delay (ps)
1	48	0.0065	2.6065	4.7	25.7	74.3	345.4
3	49	0.0065	2.6267	4.7	25.7	74.3	345.4
4	30	0.0065	2.6329	4.7	25.7	74.3	345.4
6	31	0.0065	2.6387	4.7	25.7	74.3	345.4
7	33	0.0065	2.661	4.8	26.6	74.3	358.7
9	34	0.0065	2.6294	4.7	25.7	74.3	345.4
10	36	0.0065	2.624	4.7	25.7	74.3	345.4
12	37	0.0065	2.638	4.7	25.7	74.3	345.4
13	18	0.0065	2.7273	4.8	26.6	74.3	358.7
15	19	0.0065	2.6708	4.8	26.6	74.3	358.7
16	21	0.0065	2.614	4.7	25.7	74.3	345.4
18	22	0.0065	2.704	4.8	26.6	74.3	358.7
19	24	0.0065	2.6464	4.8	26.6	74.3	358.7



Device Pin No.	Connector Pin No.	Trace Width (inches)	Length (inches)	Capacitance (pF)	Inductance (nH)	Impedance ( $\Omega$ )	Line Delay (ps)
20	25	0.0065	2.653	4.8	26.6	74.3	358.7
22	10	0.0065	2.76	5.0	27.6	74.3	372.0
23	11	0.0065	2.6717	4.8	26.6	74.3	358.7
25	8	0.0065	2.6975	4.8	26.6	74.3	358.7
26	13	0.0065	2.6953	4.8	26.6	74.3	358.7
44	42	0.0065	2.6616	4.8	26.6	74.3	358.7
45	43	0.0065	2.6482	4.8	26.6	74.3	358.7
47	45	0.0065	2.6845	4.8	26.6	74.3	358.7
48	46	0.0065	2.6441	4.7	25.7	74.3	345.4
32	23	0.015	0.6804	1.9	4.8	50.8	94.2
33	22	0.015	0.6828	1.9	4.8	50.8	94.5
34	7	0.015	0.6804	1.9	4.8	50.8	94.2
35	6	0.015	0.6991	1.9	4.9	50.8	96.8
38	5	0.015	0.6894	1.9	4.8	50.8	95.4
39	4	0.015	0.6833	1.9	4.8	50.8	94.6
40	15	0.015	0.6899	1.9	4.9	50.8	95.5
41	14	0.015	0.7026	1.9	4.9	50.8	97.3

Note: All values presented in this table are theoretical calculated values and may not reflect actual measured parameters.

Table 4. LVDS Serdes 48 Receiver PCB Transmission Line Characteristics

Device Pin No.	Connector Pin No.	Trace Width (inches)	Length (inches)	Capacitance (pF)	Inductance (nH)	Impedance ( $\Omega$ )	Line Delay (ps)
1	25	0.0065	2.76	5.0	27.6	74.3	372.0
2	10	0.0065	2.47	4.4	24.4	74.3	328.2
4	11	0.0065	3.04	5.4	30.0	74.3	403.9
5	8	0.0065	2.63	4.7	26.0	74.3	349.4
23	13	0.0065	2.63	4.7	26.0	74.3	349.4
24	42	0.0065	2.66	4.8	26.3	74.3	353.4
26	43	0.0065	2.62	4.7	25.9	74.3	348.1
27	45	0.0065	2.71	4.8	26.7	74.3	360.0
29	46	0.0065	2.64	4.7	26.1	74.3	350.7
30	48	0.0065	2.56	4.6	25.3	74.3	340.1
31	49	0.0065	2.69	4.8	26.5	74.3	357.4
33	30	0.0065	2.56	4.6	25.3	74.3	340.1
34	31	0.0065	2.71	4.8	26.7	74.3	360.0
35	33	0.0065	2.51	4.7	24.8	74.3	333.5
37	34	0.0065	2.54	4.5	25.1	74.3	337.5
39	36	0.0065	2.5	4.5	24.7	74.3	332.1
40	37	0.0065	2.58	4.6	25.4	74.3	341.4
41	18	0.0065	2.63	4.7	26.0	74.3	349.4
43	19	0.0065	2.57	4.6	25.4	74.3	341.4
45	21	0.0065	2.53	4.5	25.0	74.3	336.1
46	22	0.0065	2.47	4.4	24.4	74.3	328.2



Device Pin No.	Connector Pin No.	Trace Width (inches)	Length (inches)	Capacitance (pF)	Inductance (nH)	Impedance ( $\Omega$ )	Line Delay (ps)
47	24	0.0065	2.52	4.5	24.9	74.3	334.8
8	13	0.015	1.2138	3.3	8.5	50.8	168.0
9	12	0.015	1.1885	3.2	8.4	50.8	164.5
10	23	0.015	1.1877	3.2	8.4	50.8	164.4
11	22	0.015	1.159	3.2	8.1	50.8	160.0
14	21	0.015	1.1718	3.2	8.2	50.8	162.2
15	20	0.015	1.162	3.2	8.2	50.8	160.8
16	5	0.015	1.1889	3.2	8.4	50.8	164.6
17	4	0.015	1.2015	3.3	8.4	50.8	166.3

Note: All values presented in this table are theoretical calculated values and may not reflect actual measured parameters.

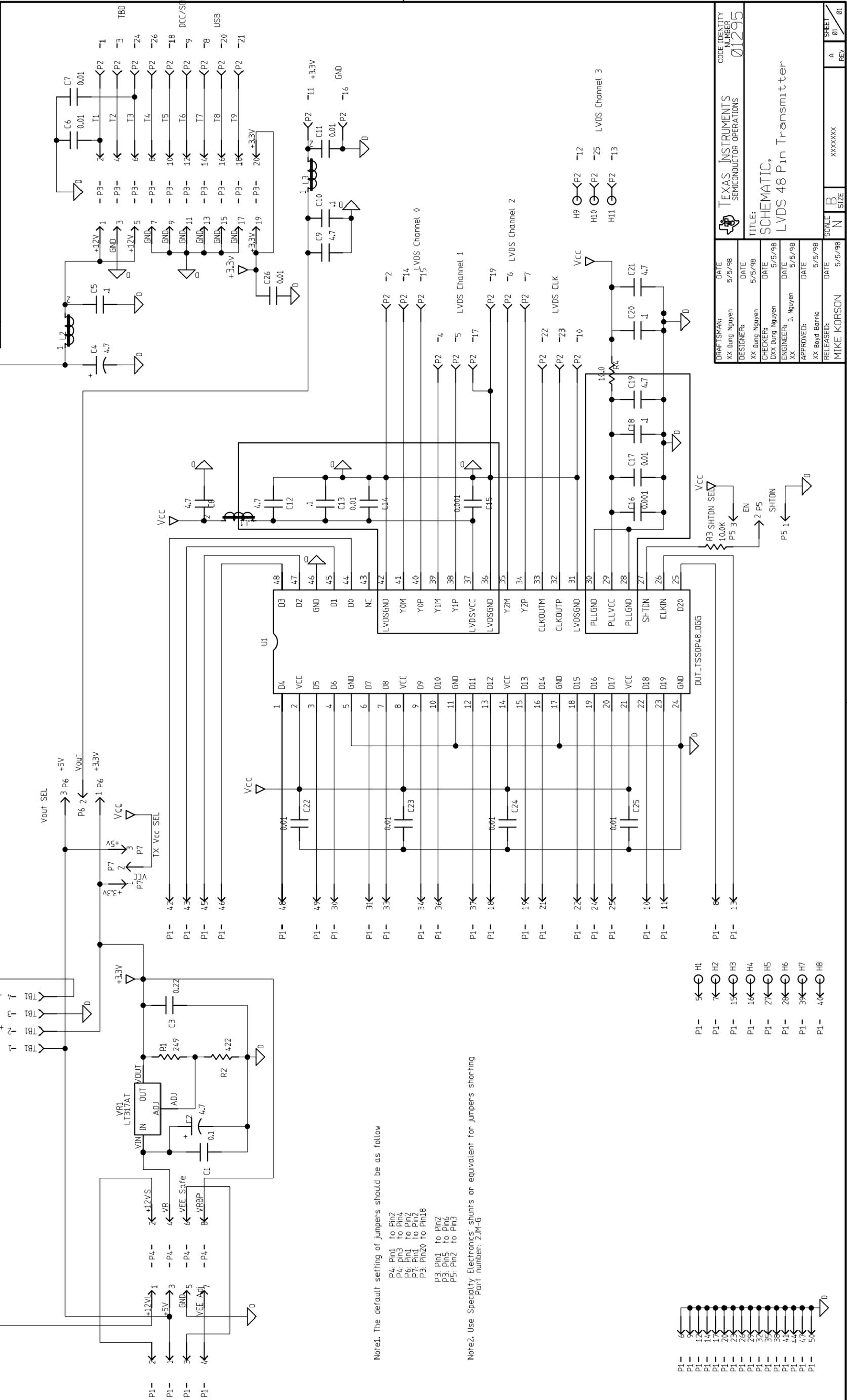
## Layer Construction for Transmitter/Receiver Boards

LAYER 1		COMP	50/75 $\Omega$
LAYER 2		GND	
LAYER 3		VCC	
LAYER 4		SOLD	50/75 $\Omega$

- Notes: 1) All cores consist of 1 oz Cu.  
 2) Trace width  
 A) 15 mils (for 50  $\Omega$ )  
 B) 6.5 mils (for 75  $\Omega$ )  
 C) 9.0 mils (for others)  
 3) Overall board thickness is 62 mils  $\pm$ 10%.  
 4) Impedance is 50  $\Omega$  and 75  $\Omega$   $\pm$ 5%.  
 5) Material is G-Tek. Dielectric constant = 3.5.

## Appendix A. Schematics, Board Layouts, and MDR Cable Assembly Specifications

This appendix contains schematics and corresponding bill of materials for the LVDS Serdes 48 pin EVM transmitter and receiver boards along with board layouts. Specifications for the MDR cable assembly are also included.



Note1. The default setting of jumpers should be as follow  
 P4: Pin1 to Pin2  
 P4: Pin3 to Pin4  
 P6: Pin1 to Pin2  
 P7: Pin1 to Pin2  
 P3: Pin20 to Pin18  
 P3: Pin1 to Pin2  
 P3: Pin5 to Pin6  
 P5: Pin2 to Pin3

Note2. Use Specialty Electronics' shunts or equivalent for jumpers shorting  
 Part number: ZJM-G



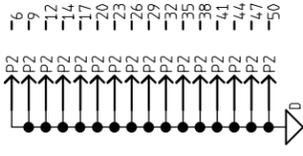
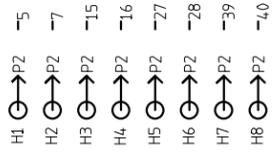
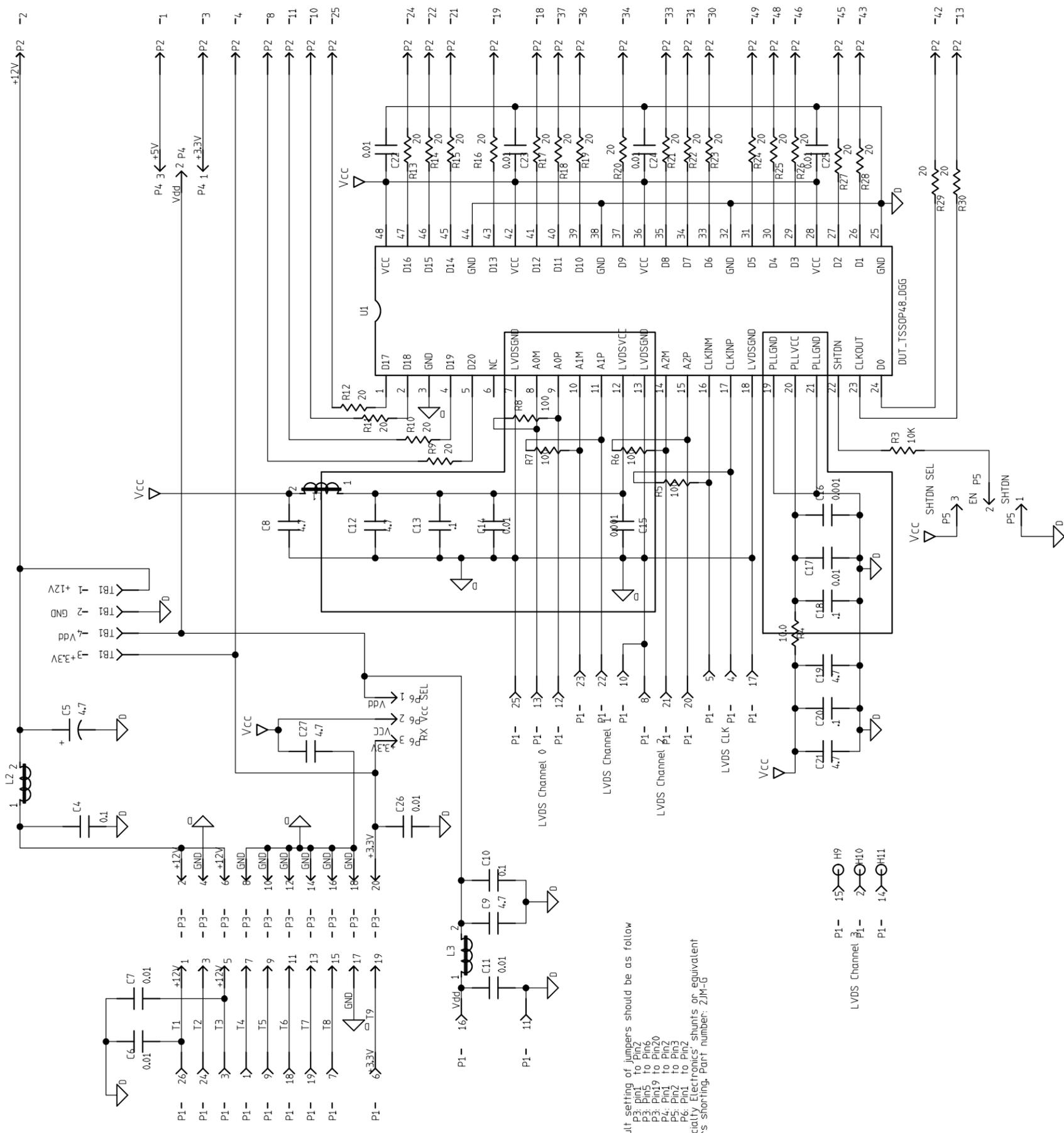
DRAFTSMAN: XX Dung Nguyen	DATE: 5/5/98	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER: 01295
DESIGNER: XX Dung Nguyen	DATE: 5/5/98	TITLE: SCHEMATIC, LVDS 48 Pin Transmitter	
CHECKER: DX Dung Nguyen	DATE: 5/5/98		
ENGINEER: N. Nguyen	DATE: 5/5/98		
APPROVED: XX Boyd Barthe	DATE: 5/5/98		
RELEASED: MIKE KORSON	DATE: 5/5/98		



Table 5. LVDS Serdes 48 Pin Transmitter Bill of Materials

Item	Qty	Mfg	Mfg Part No.	Ref Des	Description	Value or Function
762	11		.040PTH	H1-H11		.040DIA Plated hole
763	1	ROHM	MCH212C104KP	C1	CAPACITOR,SMT0805	25 V, 10%, 0.1 $\mu$ F, 0805
764	2	PANASONIC	ECS-T1DX475R	C2,C4	CAPACITOR,SMT,TANT	20%, 20 V, 4.7 $\mu$ F
765	5 *	RUTILCON	LMK316BJ475ML-B	C8,C9,C12,C19 C21	CAPACITOR,SMT1206	10 V, 20%, 4.7 $\mu$ F
766	5 *	AVX	08051C104JATMA	C5,C10,C13,C1 8C20	CAPACITOR,SMT0805	100 V, 5%, 0.1 $\mu$ F
767	1	AVX	12063C224JATMA	C3	CAPACITOR,SMT1206	25 V, 5%, 0.22 $\mu$ F
768	2	AVX	06033G102JATMA	C15,C16	CAPACITOR,SMT0603	25 V, 5%, 0.001 $\mu$ F
769	10 * *	AVX	06033G103JATMA	C6,C7,C11,C14 C17,C22,C23 C24-C26	CAPACITOR,SMT0603	25 V, 5%, 0.01 $\mu$ F
770	1	3M	10226-1210 VE	P2	CONNECTOR,SMT,26PIN	MINI D RIBBON BOARD RA RE
771	1	3M	30350-6002HB	P1	CONNECTOR,,.1X.1	LOW PROFILE HEADER
772	3	STEWART	HZ_0805_E_601_R	L1-L3	FILTER,SMT,0805	FERRITE,0805
773	1	SAMTEC	TSW-104-07-G-D	P4	HEADER,2X4,.1CTR	HEADER, 2X4, .1CTR
774	1	SAMTEC	TSW-110-07-G-D	P3	HEADER,2X10,.1CTRS	HEADER 2X 10 .1CTR
775	3	ANY	HEADER,MALE,3PI	P5-P7	HEADER	MALE,3PIN,.10 OCC
776	1	LINEAR	LT317AT	VR1	IC,3P,TO220	3 TERMINAL POSITIVE REGU
777	1		DUT_TSSOP48_DGG	U1	IC,TSSOP,48P	DUT TSSOP 48PIN DGG PKG
778	1	DALE	CRCW080510R0F	R4	RESISTOR,SM,1/10w,1%	10.0 OHM
779	1	DALE	CRCW08051002F	R3	RESISTOR,SM,1/10w,1%	10.0K OHM
780	1	DALE	CRCW0603249F	R1	RESISTOR,SMT,0603	249 OHM
781	1	DALE	CRCW0603422F	R2	RESISTOR,SMT,0603	422 OHM
782	1	ON-SHORE TECHN	ED1516-ND	TB1	TERMINAL BLOCK	TERMINAL BLOCK 4 POSITION

Total Part Count: 54  
Total Parts Cost: 0



Note1. The default setting of jumpers should be as follow  
 P3: pin1 to Pin2  
 P3: pin9 to Pin20  
 P4: pin1 to Pin2  
 P5: pin2 to Pin3  
 P6: pin1 to Pin2  
 for jumper's shorting. Part number: 2JM-G

Note2. Use Specialty Electronics' shunts or equivalent for jumper's shorting. Part number: 2JM-G

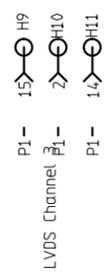
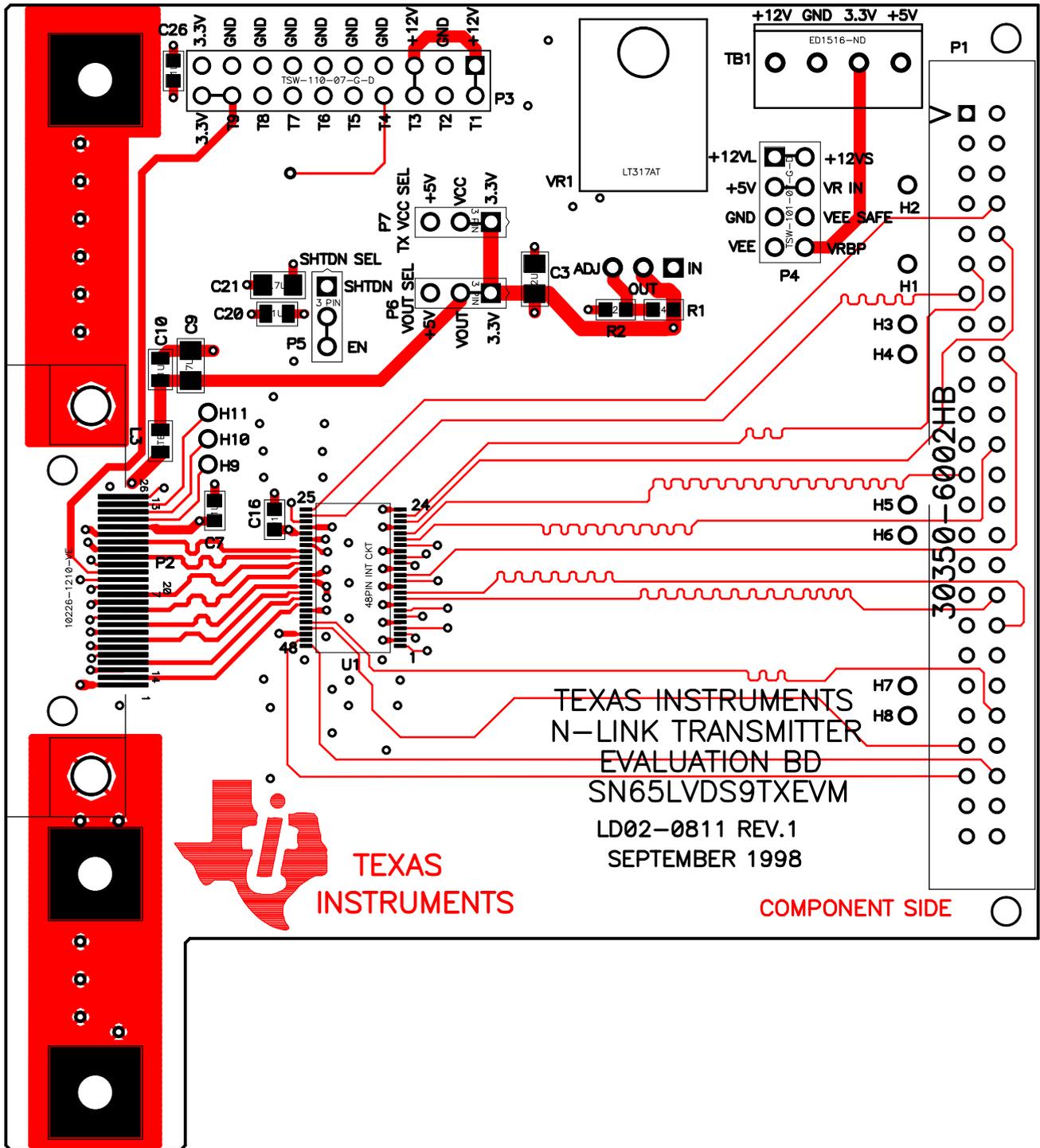




Table 6. LVDS Serdes 48 Pin Receiver Bill of Materials

Item	Qty	Mfg	Mfg Part No.	Ref Des	Description	Value or Function
84	11		.040PTH	H1-H11		.040DIA Plated hole
85	1	PANASONIC	ECS-T1DX475R	C5	CAPACITOR,SMT,TANT	20%, 20 V, 4.7 $\mu$ F
86	6 *	RUTILCON	LMK316BJ475ML-B	C8,C9,C12,C19 C21,C27	CAPACITOR,SMT1206	10 V, 20%, 4.7 $\mu$ F
87	5 *	AVX	08051C104JATMA	C4,C10,C13,C18 C20	CAPACITOR,SMT0805	100 V, 5%, .1 $\mu$ F
88	2	AVX	06033G102JATMA	C15,C16	CAPACITOR,SMT0603	25 V,5%, 0.001 $\mu$ F
89	10 * *	AVX	06033G103JATMA	C6,C7,C11,C14 C17,C22,C23 C24-C26	CAPACITOR,SMT0603	25 V,5%, 0.01 $\mu$ F
90	1	3M	10226-1210 VE	P1	CONNECTOR,SMT,26PIN	MINI D RIBBON BOARD RA RE
91	1	3M	30350-6002HB	P2	CONNECTOR, .1X.1	LOW PROFILE HEADER
92	3	STEWART	HZ_0805_E_601_R	L1-L3	FILTER,SMT,0805	FERRITE,0805
93	1	SAMTEC	TSW-110-07-G-D	P3	HEADER,2X10,.1CTRS	HEADER 2X 10 .1CTR
94	3	ANY	HEADER,MALE,3PI	P4-P6	HEADER	MALE,3PIN,.100 CC
95	1		DUT_TSSOP48_DGG	U1	IC,TSSOP,48P	DUT TSSOP 48PIN DGG PKG
96	1	DALE	CRCW080510R0F	R4	RESISTOR,SM,1/10w,1%	10.0 OHM
97	4	PANASONIC	ERJ-2GEJ101	R5-R8	RESISTOR,SMT0402	+/-1%,100
98	1	PANASONIC	ERJ-2GEJ103	R3	RESISTOR,SMT0402	+/-5%,10K
99	22	PANASONIC	ERJ-2GEJ200	R9-R30	RESISTOR,SMT0402	+/-5%,20
100	1	ON-SHORE TECHN	ED1516-ND	TB1	TERMINAL BLOCK	TERMINAL BLOCK 4 POSITION

Total Part Count: 74  
Total Parts Cost: 0

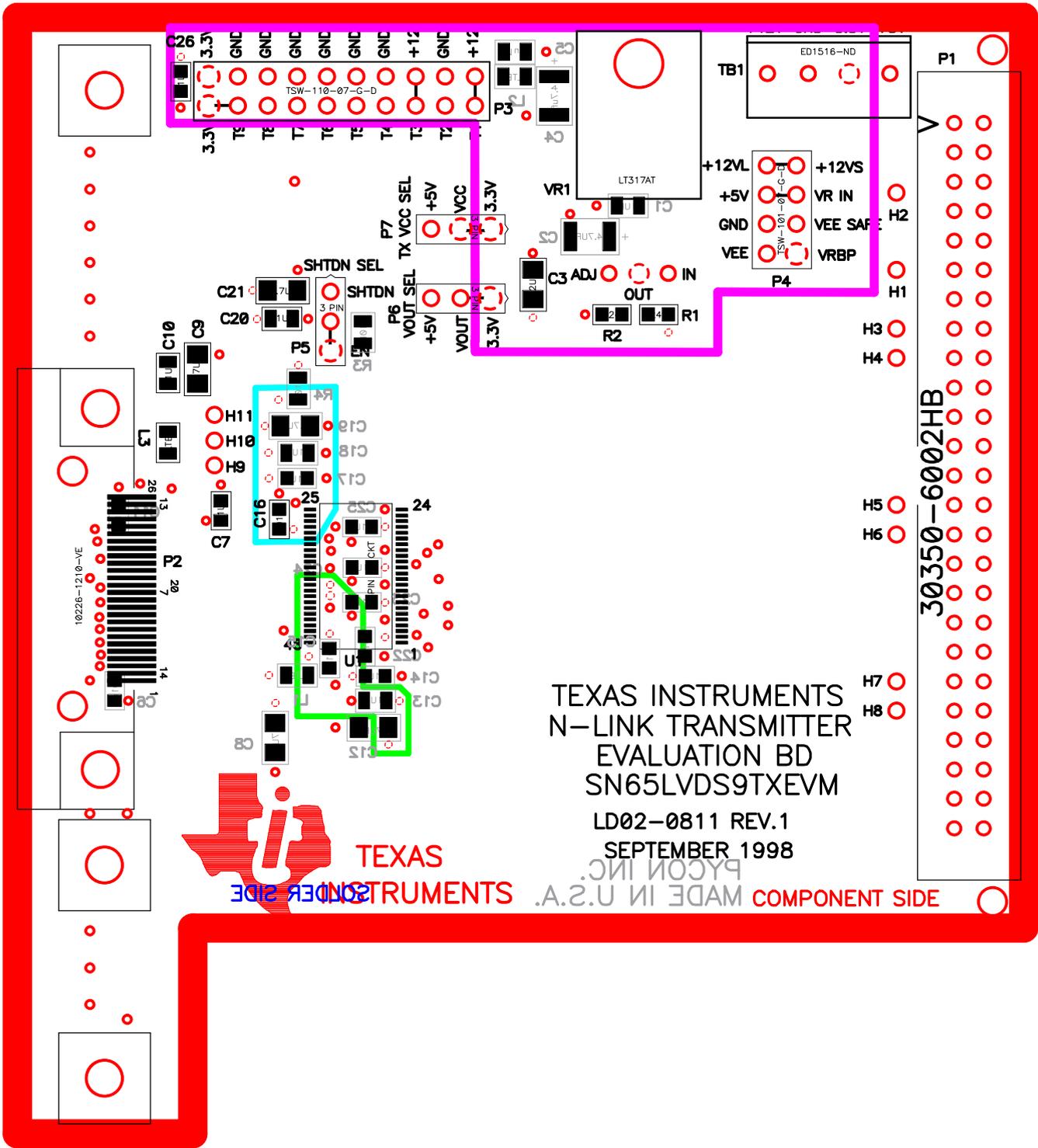


TEXAS  
INSTRUMENTS

TEXAS INSTRUMENTS  
N-LINK TRANSMITTER  
EVALUATION BD  
SN65LVDS9TXEVM

LD02-0811 REV.1  
SEPTEMBER 1998

COMPLEMENT SIDE



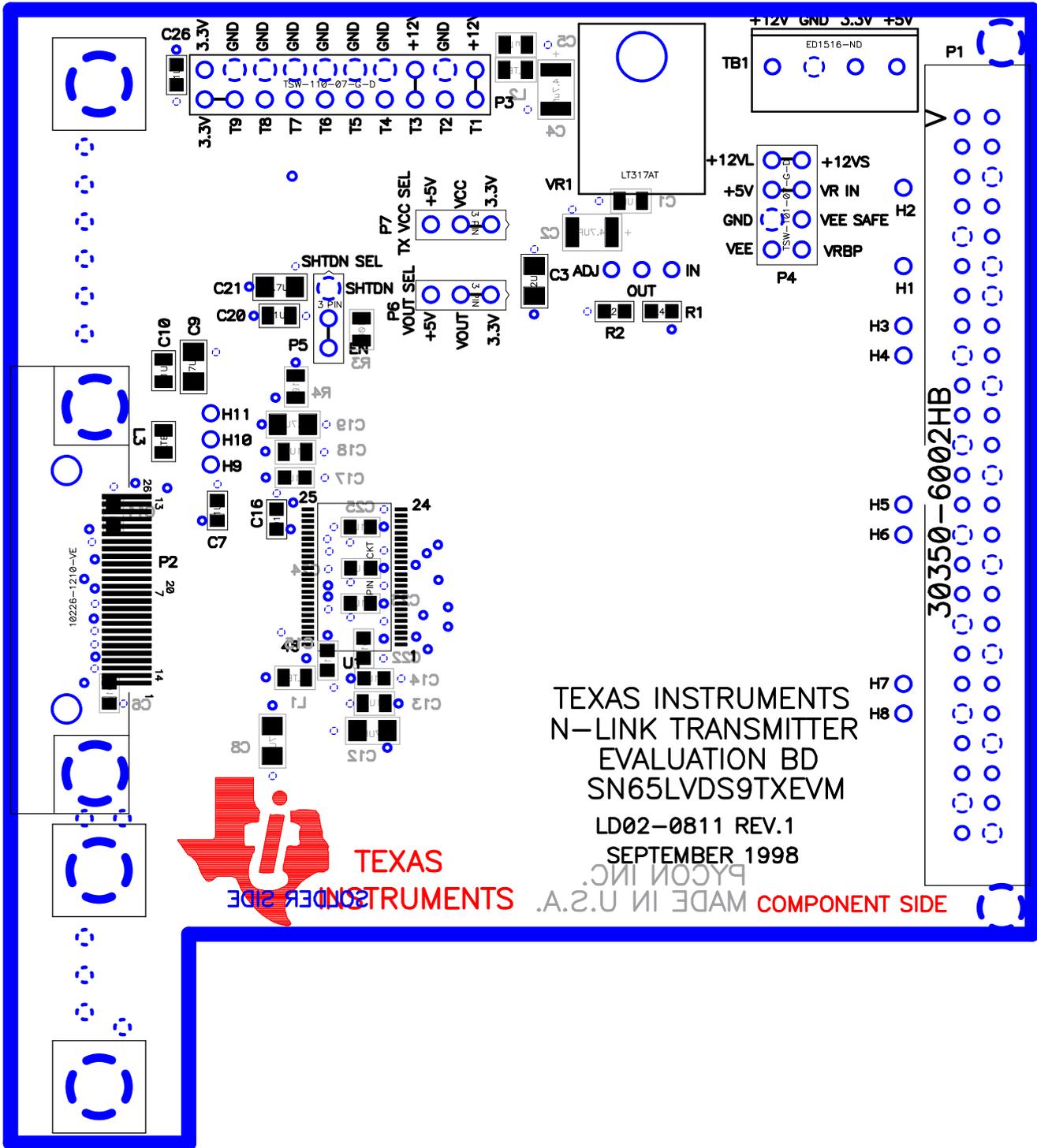
TEXAS INSTRUMENTS  
 N-LINK TRANSMITTER  
 EVALUATION BD  
 SN65LVDS9TXEVM

LD02-0811 REV.1  
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30350-6002HB



TEXAS INSTRUMENTS  
 N-LINK TRANSMITTER  
 EVALUATION BD  
 SN65LVDS9TXEVM

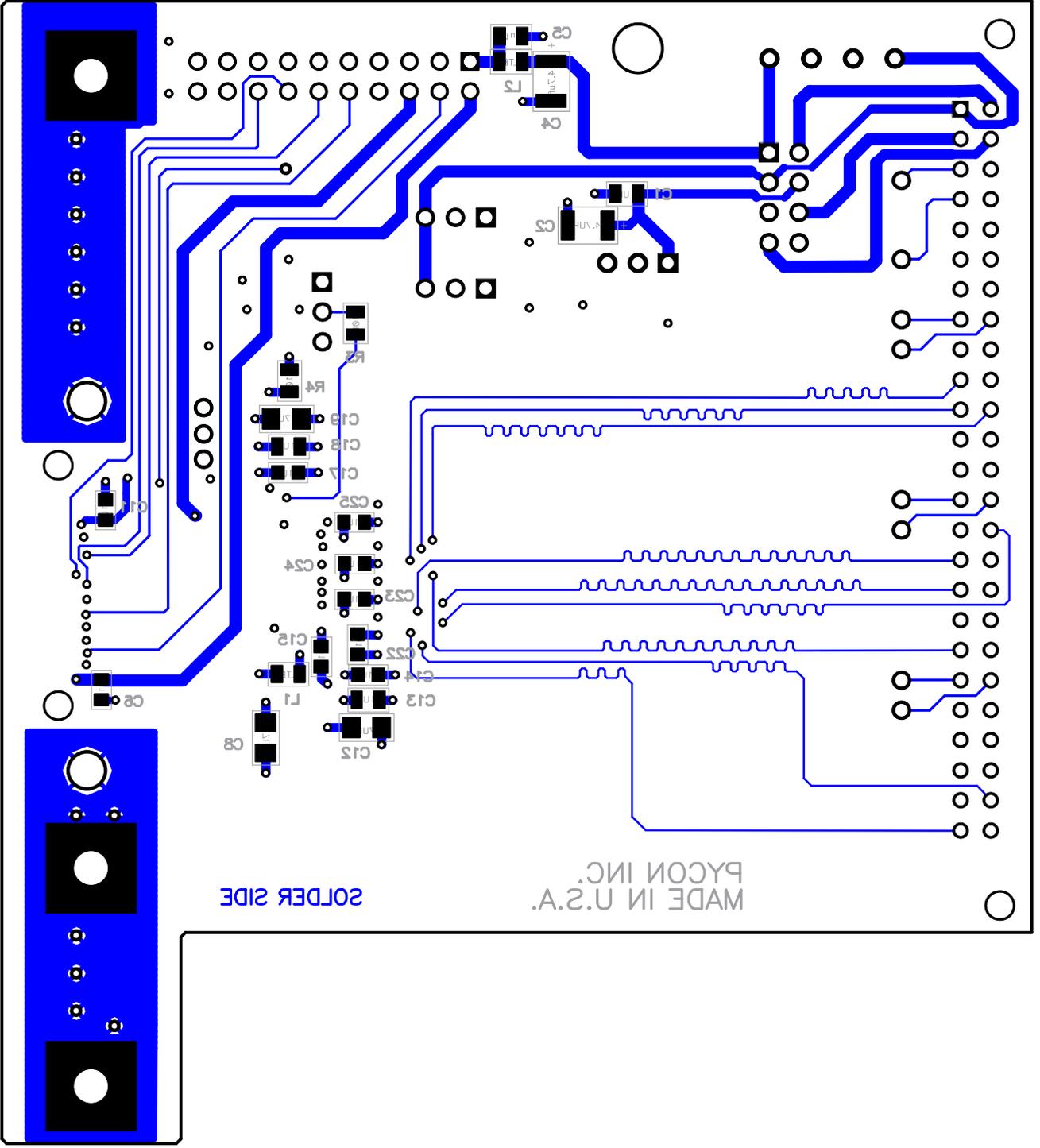
LD02-0811 REV.1  
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TEXAS  
 INSTRUMENTS

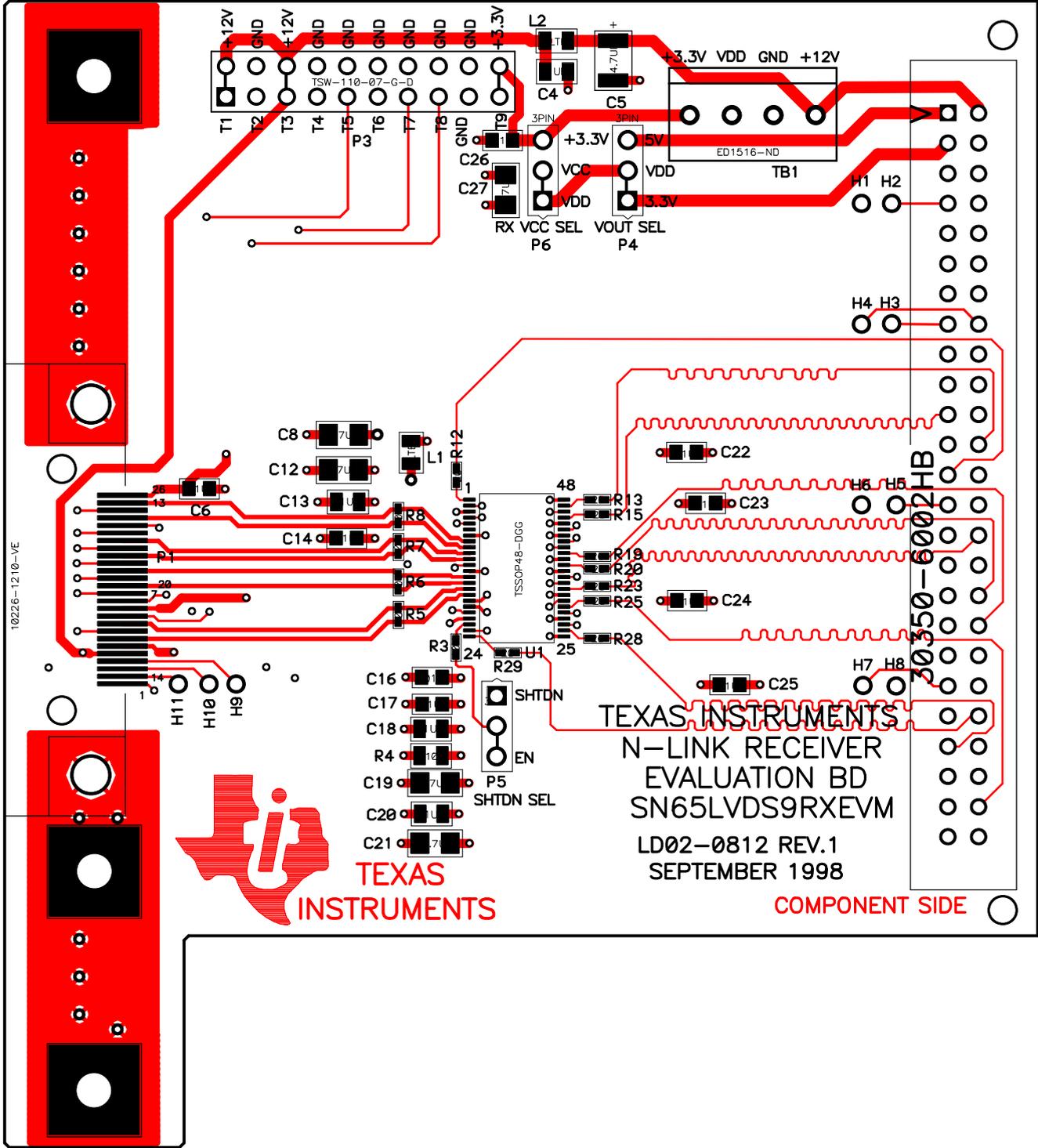
COMPONENT SIDE

MADE IN U.S.A.  
 PYCON INC.



SOLDER SIDE

MADE IN U.S.A.  
PYCON INC.



10226-1210-VE

30350-6002HB

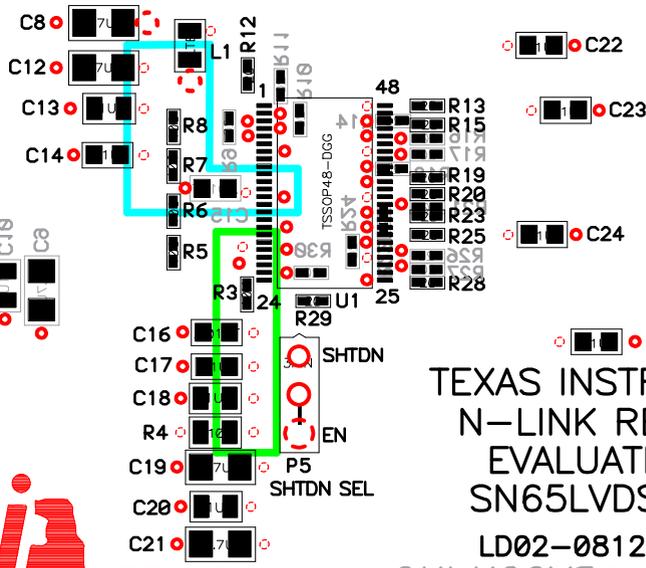
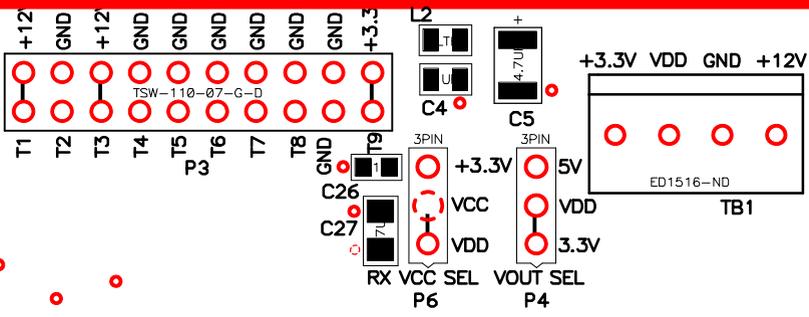


**TEXAS  
INSTRUMENTS**

**TEXAS INSTRUMENTS**  
**N-LINK RECEIVER**  
**EVALUATION BD**  
**SN65LVDS9RXEVM**  
 LD02-0812 REV.1  
 SEPTEMBER 1998

**COMPONENT SIDE**

10228-12.10-VE



TEXAS INSTRUMENTS  
 N-LINK RECEIVER  
 EVALUATION BD  
 SN65LVDS9RXEVM  
 LD02-0812 REV.1  
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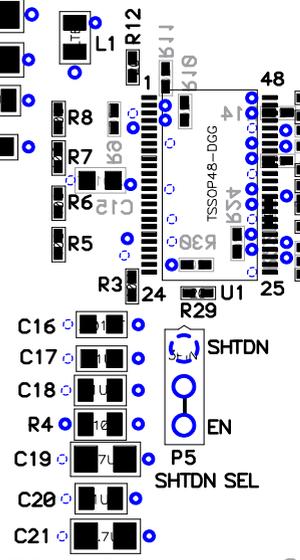
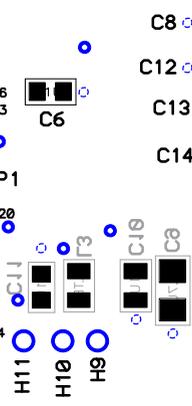
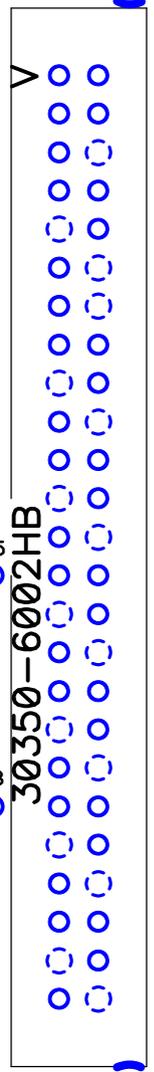
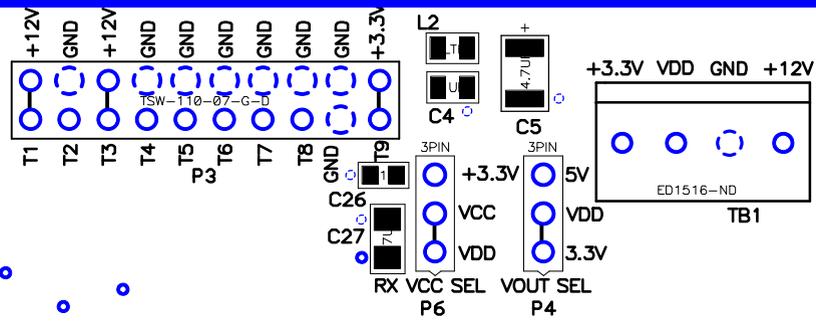
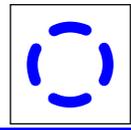
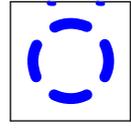
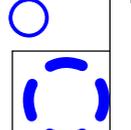
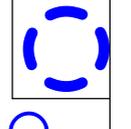
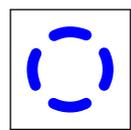
ORDER SIDE

TEXAS INSTRUMENTS

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COMPONENT SIDE

10228-1210-VE



TEXAS INSTRUMENTS  
 N-LINK RECEIVER  
 EVALUATION BD  
 SN65LVDS9RXEVM  
 LD02-0812 REV.1  
 SEPTEMBER 1998



TEXAS INSTRUMENTS

MADE IN U.S.A. (KEMET)

COMPONENT SIDE



# .050" Mini D Ribbon (MDR) Cable Assembly

High Performance Digital Transmission System — 26 to 26 Position

14526-EZ8B-XXX-07C



148

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Date Issued: June 3, 1998

TS-0757-08  
Sheet 1 of 4

## Physical

### Connector Contact Plating

Wiping Area: 30  $\mu$ " [ 0.76  $\mu$ m ] Min. Gold

### Shell

Color: Parchment/Beige

Material: Acrylonitrile Butadiene Styrene (ABS)

### Cable

Color: Parchment/Beige

Jacket Material: Polyvinyl Chloride (PVC)

## Electrical

**Voltage Rating:** 30 V

**Current Rating:** 1 A

**Insulation Resistance:**  $> 5 \times 10^8 \Omega$  at 500 Vdc

**Withstanding Voltage:** 500 Vrms for 1 minute

### Individually Shielded Twisted Pairs

**Characteristic Impedance:**  $100 \pm 10 \Omega$

**Conductor Size:** 28 AWG Stranded

**Propagation Velocity:** 1.25 ns/ft [ 4.1 ns/m ]

## Environmental

**Temperature Rating:**  $-20^\circ\text{C}$  to  $+75^\circ\text{C}$

**Flammability Rating:** N.E.C. 725, CL2

UL File No.: E86982

### 3M Electronic Products Division

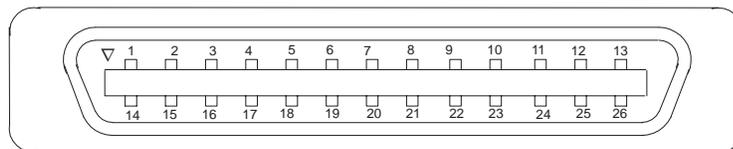
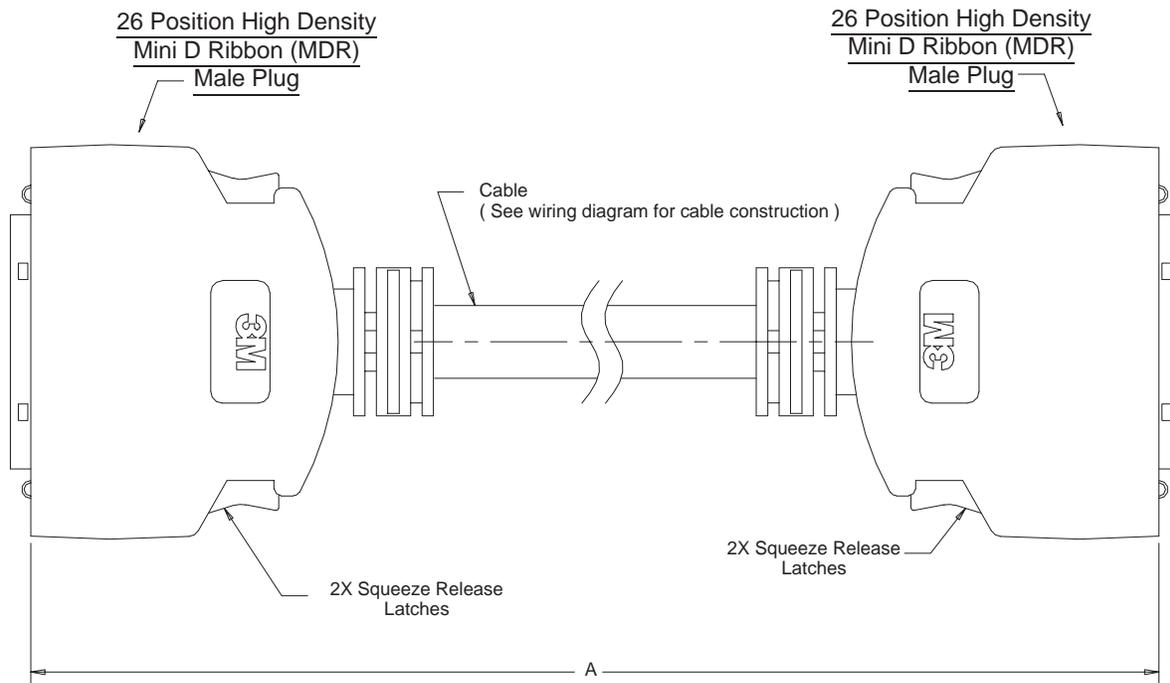
6801 River Place Blvd.  
Austin, TX 78726-9000

For technical, sales or ordering information call  
**800-225-5373**

# .050" Mini D Ribbon (MDR) Cable Assembly

High Performance Digital Transmission System — 26 to 26 Position

14526-EZ8B-XXX-07C



MDR 26 Position Plug  
( Both Ends )



## Ordering Information

**14526-EZ8B-XXX-07C**

Length see Dim A  
 060 = 2 ft.  
 200 = 2 meters  
 300 = 3 meters  
 500 = 5 meters  
 A00 = 10 meters

Note: Call 3M for details on custom polarizing keys for receptacle and plugs.

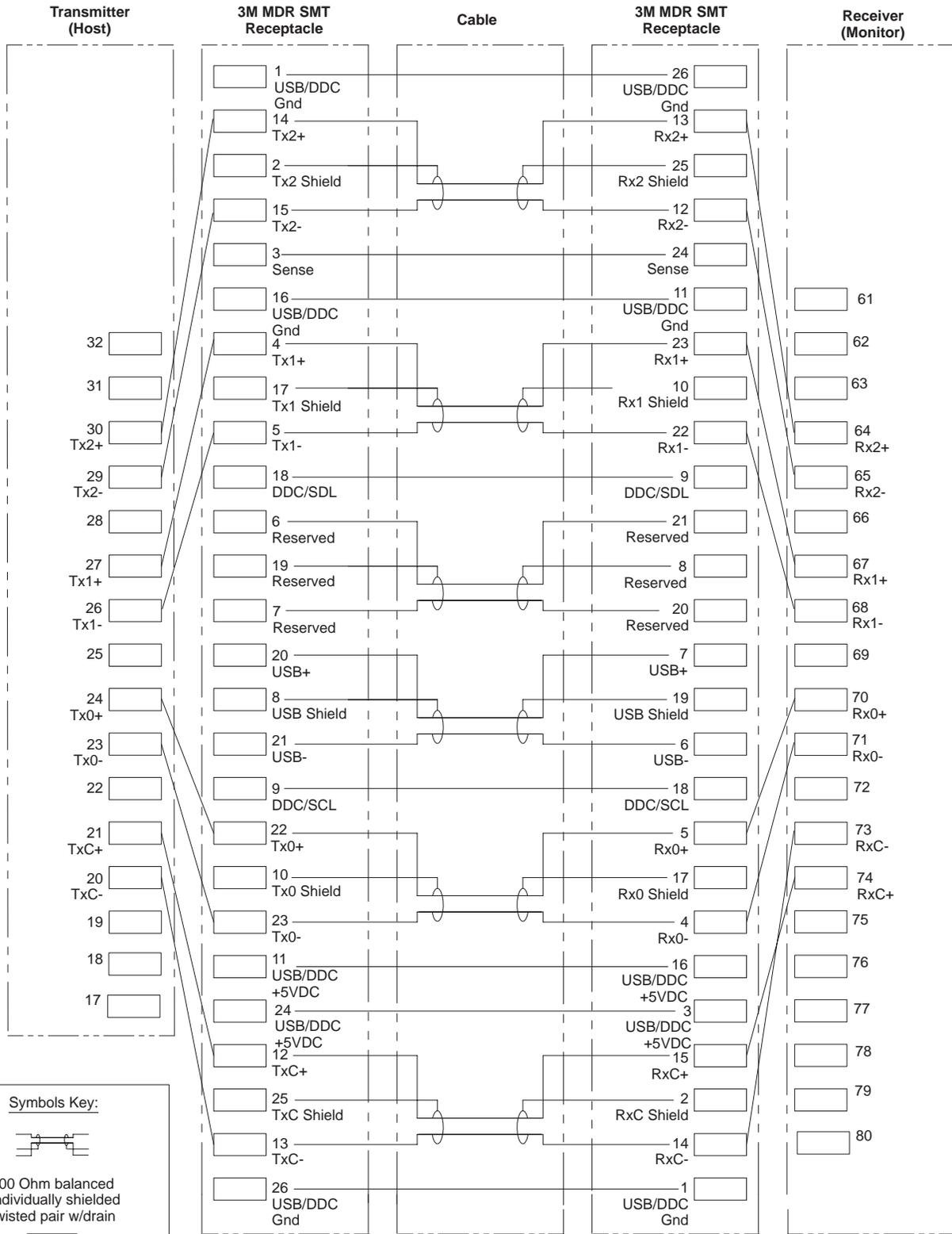
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 Sheet 2 of 4

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For technical, sales or ordering information call  
**800-225-5373**

**MDR 26 Pin, PanelLink™ /TMDS™ Pinout P26-7, Version 9.3 Cable**



**Symbols Key:**



100 Ohm balanced individually shielded twisted pair w/drain

- 28 AWG insulated conductor

PanelLink and TMDS are trademarks of Silicon Image, Inc.

TS-0757-08  
 Sheet 3 of 4

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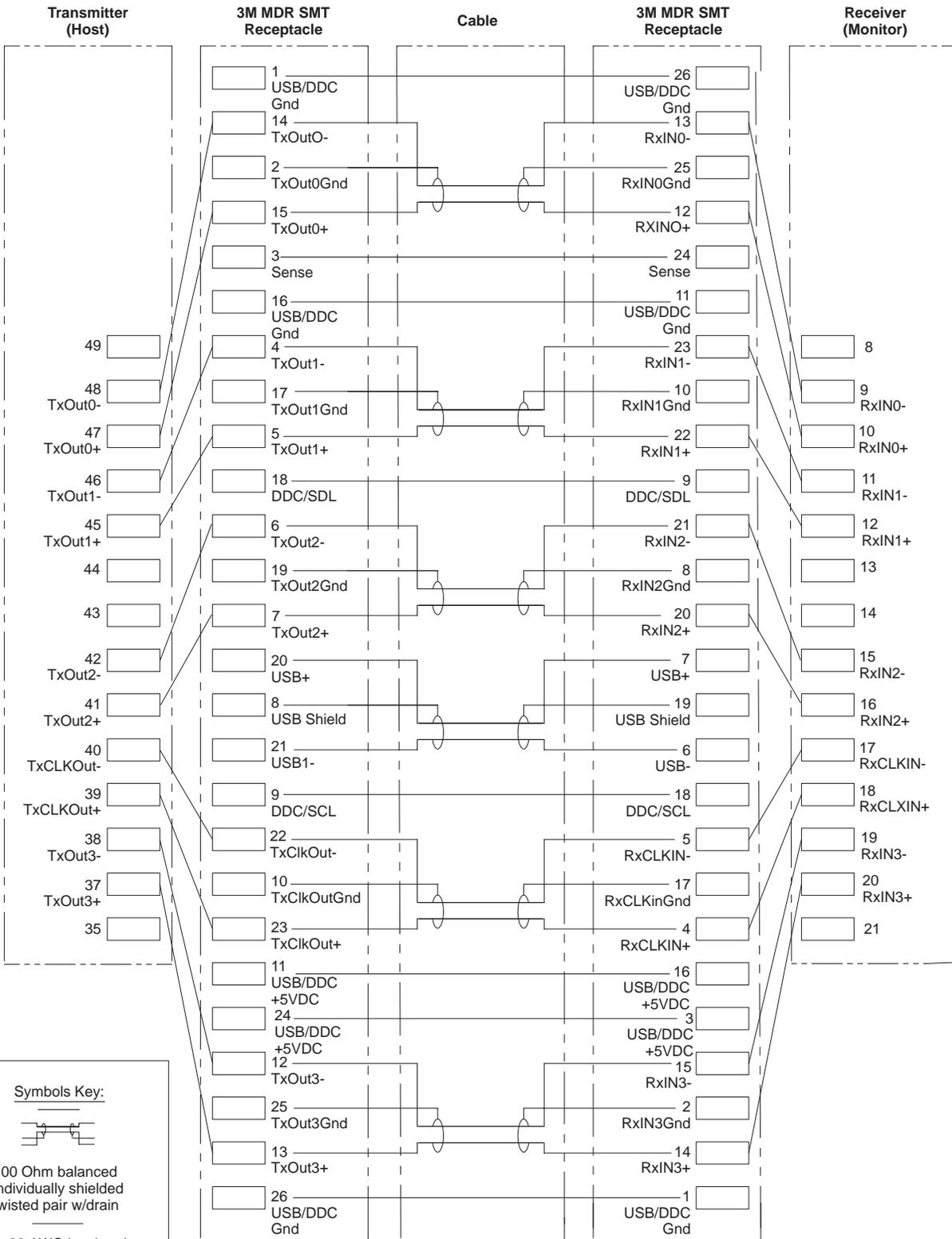
For technical, sales or ordering information call  
**800-225-5373**

# .050" Mini D Ribbon (MDR) Cable Assembly

FPD Link™ High Performance Digital Transmission System

14526-EZ8B-XXX-07C

## MDR 26 Pin, FPD Link Pinout F26-7, Version 9.3 Cable



FPD Link™ is a registered trademark of National Semiconductor Inc.

TS-0757-08  
Sheet 4 of 4

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